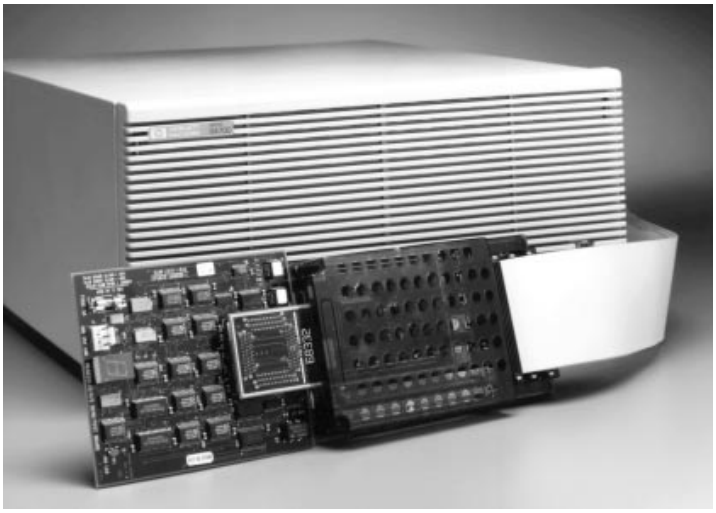
HEWLETT PACKARD

HP 64782 Emulators for Motorola 68331/332/ F333/334/336 Microcontrollers

Product Overview

Design, debug, and integrate real-time embedded systems

Hewlett-Packard has the microprocessor development solutions that you need to meet time-to-market and quality goals for Motorola 68331, 68332, 68F333, 68334, and 68336 microprocessor-based designs.



HP 64782 emulators come with zero to 8 Mbytes of emulation memory and a 6833x processor in the emula-tion pod. They support all of the standard emulation features, such as real-time trace and symbolic debug.

The emulator cards plug into a modular cardcage, which connects to your host via RS-232, RS-422, or LAN. Easy-to-use interfaces are offered on IBM-compatible PCs, Sun SPARCstations, and HP 9000 Series 300/400/700 workstations. Additionally, the cardcage's firmware-resident interface can talk to any ASCII terminal.

Designers are assured of a full line of support with modular emulation tools and software support on a wide range of platforms. Hewlett-Packard has integrated the emulator with code development, debug, emulation, software performance analysis, and software test verification into a comprehensive package that will meet your embedded design requirements. You have the choice of selecting the entire devel-opment package or only the parts that you need at a specific time.

For PC-hosted embedded development, a real-time C debugger user interface combines the ease of use of a full Microsoft Windows with HP 64700's transparent, real-time emulation. This allows you to debug embedded C programs at the source level, while your target runs at full speed.

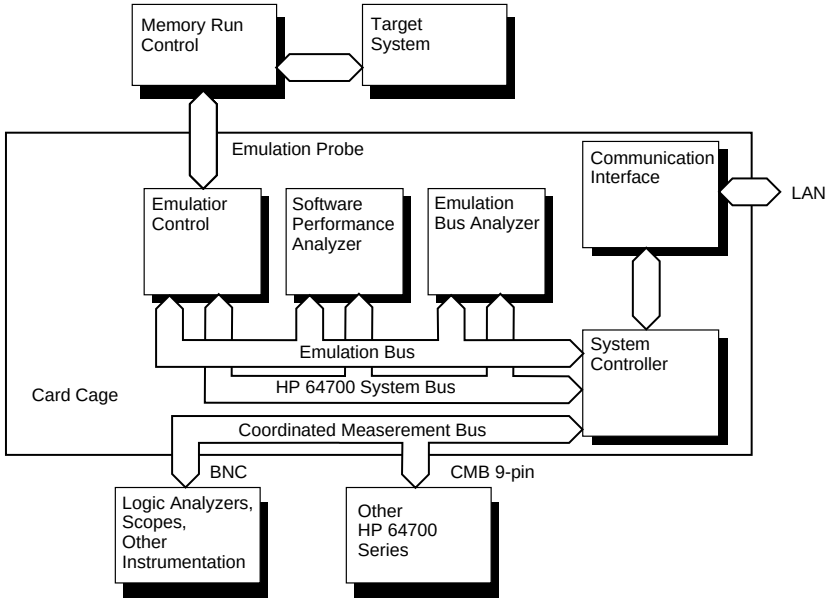
Workstation-hosted embedded development is supported with the X/Motif-based HP Embedded Debug Environment, an integrated suite of tools that span the entire software development process. The environment provides easy-to-use measurement capabilities ranging from real-time, nonintrusive analysis to high-level C and C++ source code debugging. In addition, this environment automatically integrates with the HP SoftBench framework to provide a complete CASE environment for embedded software development.

MOTOROLA 68Z 68K DEVELOPER PROGRAM

HP is a Platinum member of the Motorola Developer Program.

Features

- 20 MHz*, zero-wait-state, and fast termination cycle operation in target memory
- 20 MHz*, zero-wait-state operation in emulation memory
- Fast termination cycle to 10 MHz in emulation memory
- Supports 3.3 V and 5 V processor versions
- Supports any user-selected configuration of the SIM (or SCIM) registers and processor pins while maintaining full emulation features such as symbolic tracing and overlay memory
- Configuration menu for easy emulator setup
- Processor-specific, on-line help in Motorola format
- Display, modification, and high-level interpreted displays of on-chip peripheral registers
- Processor and emulator configuration is cross checked for inconsistencies and incompatible selections; understandable error and warning messages are given
- Reset mode configuration can be target system or emulator driven; either source is included in configuration cross checking
- Reads processor registers and automatically generates startup code
- Customizable foreground monitor
- Background-style monitor uses BDM mode
- Internal 32.768 kHz crystal or external oscillator clock modes supported
- 36-inch probe cable terminating in an active probe
- Unlimited software execution breakpoints



HP 64700 Series modular architecture offers a selection of emulators, emulation bus analyzers, optional software performance analyzer, and other tools.

- Multiprocessor emulation: synchronous start of up to 32 emulators
- Cross triggering from another emulator, logic analyzer, or oscilloscope

Emulation bus analyzer

- 80 channels available with trace buffer depths of 1K, 8K, 64K, or 256K
- Postprocessed software-based dequeued trace with symbols and source lines
- Eight events, each consisting of address, status, and data comparators
- Events may be sequenced eight levels deep
- Timing and state counts
- Prestore capability

Emulation memory

- The entire emulation memory is dual-ported, which allows modification and display without processor interruption
- 256 Kbyte, 512 Kbyte, 1 Mbyte, 1.25 Mbyte, 2 Mbyte, 4 Mbyte, 4.25 Mbyte, 5 Mbyte, and 8 Mbyte memory configurations
- Mapping resolution to 256 bytes

Software support

- Real-time operating system measurement tools
- HP language tool chain includes C compiler, assembler, linker, debugger/simulator, debugger/emulator, and branch validator
- Operates with the real-time, software performance analyzer
- Real-time C debugger for PC-hosted development*
- Support for IEEE-695, HP OMF, Motorola S record and extended Tek HEX file formats (symbols supported with IEEE-695 and HP OMF)

*Contact your HP 64000 Field Engineer for the latest configuration information, supported processor speeds, QFP adapter set availability, and software options.

Cardcage

The cardcage is the basis for modular emulators and analyzers. It can be disassembled and reassembled easily for cost-saving reconfiguration to support 8-, 16-, and 32-bit processors.

The cardcage contains a combination RS-232-C/RS-422 serial port with a standard 25-pin serial con-nector. RS-422 can be programmed to operate at rates up to 460K baud.

Networking

In many embedded designs, it is not possible for each member of a design team to have a target system and an emulator. This makes it essential to have remote access from a networked host. The HP 64700 series emulators offer a LAN connection so that you are able to share a central emulator and target from either a PC or work-station. Not only can team members share a common emulator and data-base, but you also have rapid file transfers at rates of up to six mega-bytes per minute for increased pro-ductivity. The cardcage connects to all popular Ethernet 802.3 networks through a 10Base2 ThinLAN BNC connector or a 15-pin AUI (attachment unit interface). TCP/IP proto-cols, LAN gateways, and ARPA/Berkeley standards are supported.

Emulation bus analysis

Emulation bus analysis provides real-time, nonintrusive analysis along with extensive triggering, tracing, and qualification features. Analysis features offer selective tracing, time tagging, prestore, and a selection of trace depths of 1K, 8K, 64K, or 256K. These comprehensive resources combine to solve both simple and complex problems.

Real-time, nonintrusive analysis is achieved through a dual-bus architecture. This allows traces to be set up and reviewed without breaking processor execution. Selective tracing of microprocessor code flow, without breaking execution, is a major strength of the HP 64700 series emulators and analyzers.

Up to eight hardware breakpoint resources, each consisting of address, data, and status event comparators, can be combined in sequential trace specifications, using “find A, followed by B...” constructs up to eight levels deep. A range comparator can be applied to address or data events at any one of these levels. The analyzer will trigger on and store all subsequent execution, or store only specified execution information.

Precise time tagging of events helps you identify discrepancies in code execution. Each event is logged into the analyzer with an execution time. Bus cycle, instruction, and module duration can be measured at full processor speeds.

Prestore assists you in pinpointing possible problem areas in your code. Prestore can determine which of several different functions is accessing a variable and is responsible for corrupting it.

Real-time emulation

The HP 64782 active probe emulators contain the microprocessor, emulation monitor, run-control circuits, and up to 8 Mbytes of dual-ported emulation memory. Each emulator includes background and foreground monitors. The background monitor uses no target address space. The foreground monitor is used for interrupt-sensitive systems or for customizing the monitor to the target system. For example, a foreground monitor can respond to target system interrupts while in a monitor idle loop.

Extensive breakpoint capabilities allow you to define where to stop the execution of code. Software breakpoints can be set up in the emulator, allowing execution to be halted at an instruction point. Real-time hardware break events increase the flexibility and power of this feature, extending functionality to include stopping at processor address, data, status points, or a combination of all three.

Flexible memory configuration

Memory modules are used for emulation memory. Two slots are available on the active probe, allowing you to plug in the amount of mem-ory you need—up to 8 Mbytes. If you initially order less than the maximum, you can easily expand by adding modules. Modules for 256 Kbytes (HP 64171/2A). 1 Mbyte (HP 64171/2B), and 4 Mbytes (HP 64173A) are available. The entire emulation memory is dual-ported with *no* timing intrusion, allowing you to display and modify critical program variables without halting the target system.

Robust symbolic support

Symbolic debugging is available when using the PC-hosted real-time C debugger, debugger/emulator, and workstation-hosted software tools. Symbolic debugging clarifies trace list interpretation by allowing you to see program symbols in the trace list. This facilitates quick identification of problems involving the interaction of software and hardware. You also can use symbols in emulation commands and expressions to simplify command entries and user interaction.

Workstation-hosted environment

The HP Embedded Debug Environment is a collection of integrated tools that assist you during software development. These tools include the emulator/analyzer user interface, debugger/emulator, debugger/simulator, advanced cross language system, HP Branch Validator, RTOS measurement tools, and the real-time software performance analyzer.

The **emulator/analyzer** tool gives you the ability to perform trace analysis, set breakpoints, and establish emulator configuration parameters. In addition, the graphical interface tool is integrated with the embedded debug environment, which coordinates high-level software debugging with low-level microprocessor run control.

The **debugger/emulator** and **debugger/simulator** share a common user interface for ease of learning. Both support data types, stack backtrace, and stack-resident local variables. The debugger/emulator also works with your code in real time and allows you to set breakpoints directly without having to switch to the emulator/analyzer.

The **advanced cross language system** includes HP's ANSI C compiler, assembler, and linker. These tools are integrated with the HP debug environment to provide a comprehensive array of features and functions that address embedded development needs. For example, the combination of the cross language system and debug environment allows you to display memory and symbolic trace information with overlaid C source. This allows you to view your target code from both a high- and low-level perspective to aid in debugging complex problems.

HP Branch Validator verifies software test effectiveness on complete hardware/software systems. This tool provides an easy-to-use environment for branch analysis that supports rapid iteration of the compile-test-analyze loop. Comprehensive reports, resulting from the branch validator sessions, provide detailed feedback on the execution of test suites.

Real-time operating system measurement tools allow you to transparently trace operating system task flow, service call activity, and measure system performance on running systems. These tools support pSOS+, VRTX32, and user-developed operating systems.

The HP debug environment supports many popular language tools from Microtec Research Inc. and Intermetrics, as well as the HP advanced cross language system of compilers, assemblers, and linkers. The debug environment also operates within the optional HP SoftBench environment, which brings advanced CASE tools and techniques to the realm of embedded software design.

Optional **software performance analysis** enables you to tune and verify the time-critical aspects of your design. These capabilities are provided at both the C source and assembly language levels. Through automated one-key setup, this system quickly identifies code bottlenecks and gathers statistics and timing information that aid in solving time-critical problems. The software performance analyzer operates with HP 9000 Series 300/400/700 workstations and Sun SPARCstations.

PC-hosted environment

The **real-time C debugger** (HP B3624A*) is a mouse-driven Microsoft Windows-based, graphical user interface for HP 64700 emulators. The debugger takes full advantage of the emulator's dual-bus architecture and dual-ported memory to perform many C and assembly debug functions while the target runs at full speed. This means that C debugger functions such as setting breakpoints, display and edit of C variables, and measurement of C program behavior can now often be performed without interrupting program execution. This traditionally could be performed only when a user program was stopped.

Terminal mode operation

A firmware-resident ASCII terminal interface is embedded in the emulator, supplying commands for all emulation and analysis features. Commands are ASCII strings; file transfers using industry-standard formats are accepted. Since a terminal can access these commands, host independence is realized.

* Contact your HP 64000 Field Engineer for the latest configuration information, supported processor speeds, QFP adapter availability, and software options.

Specifications and Characteristics

Processor compatibility

The HP 64782 emulator supports the Motorola 6833x family microprocessors operating at clock speeds up to 33 MHz.* The emulator supports both 5V and 3.3V operation. The emulator terminates in an AMP socket, and it can be plugged into a PQFP target system using optional accessories.

Environmental

Temperature: operating, 0° to +40°C (+32° to +104°F); nonoperating, –40°C to +70°C (–40°F to +158°F).

Altitude: operating/nonoperating 4600 m (15 000 ft).

Relative humidity: 15% to 95%.

Regulatory compliance
(When installed in HP 64700 cardcage)

Electromagnetic interference:
CISPR 11:1990/EN 55011 (1991): group 1 class A
IEC 801-2:1991/EN 50082-1 (1992): 4 kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m, 80% modulation, 26 MHz–1000 MHz
IEC 801-4:1988/EN 50082-1 (1992): 0.5 kV signal lines, 1 kV power lines

Safety: self-certified to UL 1244, IEC 1010-1, CSA-C22.2 no. 231 Series-M89

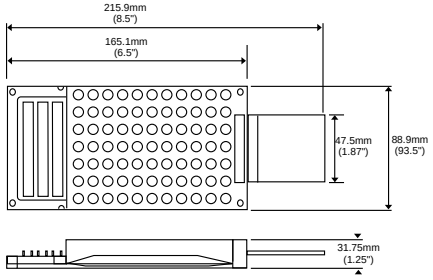
Physical

Emulator dimensions: 173 mm height x 325 mm width x 389 mm depth (6.8 in. x 12.8 in. x 15.3 in.)

Cable length: emulation control card to probe, approximately 914 mm (36 inches).

Probe weight: 0.3 kg (10 oz).

Probe dimensions:



Electrical

Maximum clock speed: 33 MHz*
(with limitations shown in the table):

	Zero Wait State	One Wait State
Target memory/ Fast termination cycle	0 to 33 MHz	N/A
Emulation memory using:		
HP 64171 (35 ns SIMM)	0 to 16.78 MHz	16.78 to 25 MHz
HP 64172 (20 ns SIMM)	0 to 25 MHz	25 to 33 MHz
HP 64173 (25 ns SIMM)	0 to 22 MHz	22 to 30 MHz

*At the time this data was printed: The MC68331 and MC68332 emulators had been tested at 20 MHz. The MC68336 emulator had been tested at 16.78 MHz. Contact your HP 64000 Field Engineer for current supported processor speeds.

DC electrical specifications

(V_{DD} and V_{DDSYN} = 5.0 Vdc ±10%, VSS = 0 Vdc)

Characteristic	Signal	Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	0.7*V_{DD}	V_{DD}+0.3	V
Input Low Voltage		V_{IL}	V_{SS}-0.3	0.2*V_{DD}	V
Undershoot			—	1.0	V
Hi-Z (Off-State) Leakage Current @ V_{IN} = GND or V_{DD}		I_{OZ}	-20	20	mA
Signal Low Input Current	$\overline{RESET}$	I_{IL}	_	0.8	mA
(V_{IL} = 0.8 V)	All other signals		—	100	mA
Signal High Input Current (V_{IH} = V_{DD})	All Signals	I_{IH}	—	50	mA
Output High Voltage					
I_{OH} = -0.8 mA, V_{DD} = 4.5 V	All Signals Except $\overline{HALT}$ and $\overline{RESET}$	V_{OH}	V_{DD}-0.8	—	V
Output Low Voltage		V_{OL}			
I_{OL} = 1.6 mA	FREEZE, $\overline{IPIPE}$, $\overline{IFETCH}$, D15-0		—	0.4	V
I_{OL} = 5.3 mA	$\overline{CSBOOT}$, $\overline{CS10}$-0, $\overline{DSACK}$[1:0], SIZ[1:0], $\overline{RMC}$, $\overline{AVEC}$, R/$\overline{W}$, $\overline{AS}$, $\overline{DS}$		—	0.4	V
I_{OL} = 15.3 mA	$\overline{HALT}$, $\overline{RESET}$		—	0.4	V
I_{OL} = 64 mA	CLKOUT		—	0.4	V
Same as 6833x Specification	Any pins not listed		—	0.4	V
Input Capacitance	$\overline{CSBOOT}$, $\overline{CS10-0}$, D15-0	C_{in}	—	50	pF
	A18-0, $\overline{DSACK}$[1:0], SIZ1-0, R/$\overline{W}$, $\overline{AS}$, $\overline{DS}$		—	30	pF
	Any pins not listed		—	20	pF
Load Capacitance		C_L	_	100	pF
Power Supply Current Drawn from Target System			—	250	mA

AC timing specifications

All specifications are the same as listed in the Motorola *MC68332 User's Manual*, except for the following.*

(V_{DD} and V_{DDSYN} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc)

		16.78 MHz		20.97 MHz		
Num	Characteristic	Min	Max	Min	Max	Unit
F1	Frequency of Operation (32.768 kHz or 4.194304 MHz crystal, as appropriate)	0.13	16.78	0.13	20.97	MHz
1	Clock Period	59.6	—	47.7	—	ns
1A	ECLK Period	476	—	381	—	ns
1B	External Clock Input Period	59.6	—	47.7	—	ns
2,3	Clock Pulse Width	21	—	16	—	ns
2A,3A	ECLK Pulse Width	236	—	183	—	ns
2B,3B	External Clock Input High/Low Time	29.8	—	23.8	—	ns
4,5	Clock Rise and Fall Time	—	5	—	5	ns
5C	CLKOUT Buffer Delay	2	5	2	5	ns
6	Clock High to Address, FC, SIZE, RMC Valid	-5	27	-5	21	ns
7	Clock High to Address, FC, SIZE, RMC High Impedance	-5	57	-5	45	ns
8	Clock High to Address, FC, SIZE, RMC Invalid	-5	—	-5	—	ns
9	Clock Low to AS, DS, CS Asserted	-3	23	-3	21	ns
9A	AS to DS or CS Asserted (Read)	-15	15	-10	10	ns
11	Address, FC, SIZE, RMC Valid to AS, CS (and DS Read) Asserted	15	—	10	—	ns
12	Clock Low to AS, DS, CS Negated	-3	27	-3	21	ns
13	AS, DS, CS Negated to Address, FC, SIZE Invalid (Address Hold)	15	—	10	—	ns
14	AS, CS (and DS Read) Width Asserted	100	—	80	—	ns
14A	DS, CS Width Asserted (Write)	45	—	36	—	ns
14B	AS, CS (and DS Read) Width Asserted (Fast Write Cycle)	40	—	32	—	ns
15	AS, DS, CS Width Negated	40	—	32	—	ns
16	Clock High to AS, DS, R/W High Impedance	—	57	—	45	ns
17	AS, DS, CS Negated to R/W Negated	15	—	10	—	ns
18	Clock High to R/W High	-5	27	-5	21	ns
20	Clock High to R/W Low	-5	27	-5	21	ns
21	R/W Asserted to AS, CS Asserted	15	—	10	—	ns
22	R/W Low to DS, CS Asserted (Write)	70	—	54	—	ns
23	Clock High to Data Out Valid	—	27	—	21	ns
24	Data Out Valid to Negating Edge of AS, CS (Fast Write Cycle)	15	—	10	—	ns
25	DS, CS Negated to Data Out Invalid (Data Out Hold)	15	—	10	—	ns
26	Data Out Valid to DS, CS Asserted (Write)	15	—	10	—	ns
27	Data In Valid to Clock Low (Data Setup)	10	—	10	—	ns
27A	Late BERR, HALT Asserted to Clock Low (Setup Time)	25	—	20	—	ns
28	AS, DS Negated to DSACK[1:0], BERR, HALT, AVEC Negated	0	80	0	60	ns
29	DS, CS Negated to Data In Invalid (Data In Hold)	0	—	0	—	ns
29A	DS, CS Negated to Data In High Impedance	—	55	—	48	ns
30	CLKOUT Low to Data In Invalid (Fast Cycle Hold)	13	—	8	—	ns
30A	CLKOUT Low to Data In High Impedance	—	88	—	70	ns
31	DSACK[1:0] Asserted to Data In Valid	—	50	—	46	ns
33	Clock Low to BG Asserted/Negated	—	27	—	21	ns
35	BR Asserted to BG Asserted (RMC Not Asserted)	1	—	1	—	t_{cyc}
37	BGACK Asserted to BG Negated	1	2	1	2	t_{cyc}
39	BG Width Negated	2	—	2	—	t_{cyc}
39A	BG Width Asserted	1	—	1	—	t_{cyc}
46	R/W Width Asserted (Write or Read)	150	—	115	—	ns
46A	R/W Width Asserted (Fast Write or Read Cycle)	90	—	70	—	ns
47A	Asynchronous Input Setup Time BR, BGACK, DSACK[1:0], BERR, AVEC, HALT	10	—	10	—	ns
47B	Asynchronous Input Hold Time	13	—	10	—	ns
48	DSACK[1:0] Asserted to BERR, HALT Asserted	—	30	—	30	ns
53	Data Out Hold from Clock High	-5	—	-5	—	ns
54	Clock High to Data Out High Impedance	—	26	—	21	ns
55	R/W Asserted to Data Bus Impedance Change	40	—	32	—	ns
56	RESET Pulse Width (Reset Instruction)	512	—	512	—	t_{cyc}
70	Clock Low to Data Bus Driven (Show)	-5	27	-5	21	ns
71	Data Setup Time to Clock Low (Show)	17	—	12	—	ns
73	BKPT Input Setup Time	n/a	n/a	n/a	n/a	ns
74	BKPT Input Hold Time	n/a	n/a	n/a	n/a	ns
75	Mode Select Setup Time	20	—	20	—	t_{cyc}
76	Mode Select Hold Time	0	—	0	—	ns
77	RESET Assertion Time	4	—	4	—	t_{cyc}
78	RESET Rise Time	—	10	—	10	t_{cyc}

*Contact your HP 64000 Field Engineer for more specific timing specifications for emulators for 68F333 and 68336.

Ordering Information

Terminal-Based Emulation System

Model	Description
64782B*	20 MHz active probe emulator for 68331 PQFP processors (includes demo board)
64782C*	20 MHz active probe emulator for 68332 PQFP processors (includes demo board)
64782D*	16.78 MHz active probe emulator for 68F333 PQFP processors (includes demo board)
64782E*	20 MHz active probe emulator for 68334G PQFP processors (includes demo board)
64782G*	16.78 MHz active probe emulator for 68336 PQFP processors (includes demo board)
64748C	Emulation control card
64704A	1K deep 80-channel emulation bus analyzer
64700B	Card cage

Emulation System Options

64172A	256 Kbyte, SRAM memory module (20 ns)
64172B	1 Mbyte, SRAM memory module (20 ns)
64173A	4 Mbyte, SRAM memory module (25 ns)
64037A	RS-422 interface card for PC compatibles
64708A	Software performance analyzer card, (supported on HP 9000 Series workstations, and Sun SPARCstations, HP B1487A software, required)
64023A	CMB cable (4m long; includes three 9-pin connectors)
64794A	8K deep 80-channel emulation bus analyzer
64794C	64K deep 80-channel emulation bus analyzer
64794D	256K deep 80-channel emulation bus analyzer
E3407A	AMP socket to 132-pin PQFP/CQFP adapter
E3433A*	144-pin PQFP adapter
64171A	256 Kbyte, SRAM memory module (35 ns)
64171B	1 Mbyte, SRAM memory module (35 ns)

Software Options for Workstations

For each software model number ordered, purchase one media option and at least one license option for each concurrent user.

B3092B	Graphical emulator/analyzer
B1466B	Debugger/simulator
B1473A	Debugger/emulator
B1487A	Software performance analyzer (requires HP 64708A analyzer card)
B1418A	Branch Validator
B3080A	Real-time operating system measurement tool for pSOS+
B3081A	Real-time operating system measurement tool for VRTX32
B3082A	Custom real-time operating system measurement tool

Advanced Cross Language Tools

B3640A	Assembler/linker
B3641A	ANSI C cross compiler

Media/License Options

Opt AAH	HP 9000 Series 300/400 manuals/media (DDS DAT tape)
Opt AAX	HP 9000 Series 300/400 manuals/media (1/4 inch cartridge tape)
Opt UBX	HP 9000 Series 300/400 single user license
Opt AAY	HP 9000 Series 700 manuals/media (DDS DAT tape)
Opt UBY	HP 9000 Series 700 single user license
Opt AAV	Sun SPARCstation manuals/media (1/4 inch cartridge tape)
Opt UBK	Sun SPARCstation single user license

Software Options for PCs

B3624A*	Real-time C debugger interface

Advanced Cross Language Tools

B3640A	Assembler/linker
B3641A	ANSI C cross compiler

Media/License Options

Opt AJ4	IBM 3 1/2" manuals/media
Opt AJ5	IBM 5 1/4" manuals/media
Opt UDY	IBM single user license

Software Support

HP provides software upgrades through the purchase of the software materials subscription (SMS) service. Contact your HP field engineer for more information.

* Contact your HP 64000 Field Engineer for the latest configuration information, supported processor speeds, QFP adapter availability, and software options.

HEWLETT PACKARD

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For more information, call your local HP sales office listed in your telephone directory, or an HP regional office listed below for the location of your nearest sales office.

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